PATENT SPECIFICATION (11) 1 506 101

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(21) Application No. 333/76 (22) Filed 6 Jan. 1976 (19)

(31) Convention Application No. 2511478 (32) Filed 15 Mar. 1975 in

(33) Fed. Rep. of Germany (DE)

(44) Complete Specification published 5 Apr. 1978

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G1A 205; 207; 372; 750; 753; 773; SS

(54) PHOTODIODE CIRCUIT

(71) We, FRANKE & HEIDECKE GmbH, a German Body Corporate, trading as Rollei-Werke Franke & Hiedecke, of 196 Salzdahlumerstrasse, Braunschweig, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a photo-diode circuit arrangement for the amplification of photo-electric current with a field effect transistor (FET) connected on the "source follower" principle and with a photo-diode connected between source and gate.

In photo optical measuring apparatus use is made of circuit arrangements in which brightness values are measured with Si-photo-diodes. Photo-diodes, however, supply very low currents and must not, in amplifier circuits, be separately loaded by other circuit elements. They are therefore placed in input circuits of transistors provided with high input resistors as impedance convertors. The measuring apparatus can be improved, in the known manner, by the use of amplifier stages with field effect transistors, as a result of their higher input resistances. In this connection particular consideration is to be given to the so-called "source follower" circuit, in which the drain is connected to a positive potential and the resistors Rs and Rg included in the source branch and in the gate branch respectively. To amplify the low photo-electric currents through a resistor placed in the source line, the latter higher current causing the output voltage in this resistor to increase, within wide limits, by the amount of the voltage change caused by the photo-diode in the gate of the FET.

Basic circuits of this kind, as regards their linearity, are relatively inadequate for high-quality measuring methods, as the current which flows through the load resistor in the source line and from which the output voltage is taken has to be controlled by the field effect transistor itself. Owing to the finite steepness of the operating characteristic of the FET the voltage change required between the gate and the source, in order to change the current within the necessary control range, is by no means negligible, in addition to which, owing to the curvature of the operating characteristic of the FET, it is not linear.

The resulting voltage fluctuations in the bias voltage in the photo-diode, moreover, also cause the disturbing influence of the intrinsic capacities of the photo-diode to take effect, thus reducing the limit frequency of the circuit.

The present invention provides an improved circuit arrangement to the type previously described, enabling the known drawbacks to be avoided and a largely constant bias voltage to be obtained in the photo-diode, thus considerably improving the linearity conditions.

According to the invention there is provided a photo-diode circuit arrangement for

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PATENT OFFICE

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In photo optical measuring apparatus use is made of circuit arrangements in which brightness values are measured with Si-photo-diodes. Photo-diodes, however, supply very low currents and must not, in amplifier circuits, be separately loaded by other circuit elements. They are therefore placed in input circuits of transistors provided with high input resistors as impedance convertors. The measuring apparatus can be improved, in the known manner, by the use of amplifier stages with field effect transistors, as a result of their higher input resistances. In this connection particular consideration is to be given to the so-called "source follower" circuit, in which the drain is connected to a positive potential and the resistors Rs and Rg included in the source branch and in the gate branch respectively. To amplify the low photo-electric currents the photo-diode is connected between the source and the gate of the FET.

If, as a result of the incidence of light, a photo-electric current flows through the photo-diode, it will produce, in the working resistor in the gate supply conductor, a voltage drop which actuates the FET. The higher current flowing through the FET will likewise enable a higher current to flow through a resistor placed in the source line, the latter higher current causing the output voltage in this resistor to increase, within wide limits, by the amount of the voltage change caused by the photo-diode in the gate of the FET.

Basic circuits of this kind, as regards their linearity, are relatively inadequate for high-quality measuring methods, as the current which flows through the load resistor in the source line and from which the output voltage is taken has to be controlled by the field effect transistor itself. Owing to the finite steepness of the operating characteristic of the FET the voltage change required between the gate and the source, in order to change the current within the necessary control range, is by no means negligible, in addition to which, owing to the curvature of the operating characteristic of the FET, it is not linear.

The resulting voltage fluctuations in the bias voltage in the photo-diode, moreover, also cause the disturbing influence of the intrinsic capacities of the photo-diode to take effect, thus reducing the limit frequency of the circuit.

The present invention provides an improved circuit arrangement to the type previously described, enabling the known drawbacks to be avoided and a largely constant bias voltage to be obtained in the photo-diode, thus considerably improving the linearity conditions.

According to the invention there is provided a photo-diode circuit arrangement for the amplification of photo-electric current, comprising: a field effect transistor connected on the "source follower" principle, a photo-diode connected between source and gate of said field effect transistor and a pnp transistor the base of which being connected with the drain and the collector with a source connection of the field effect transistor and the emitter of which being con-

nected to the drain supply line.

This ensures that a change caused in the gate voltage by the photo-electric current of the photo-diode will lead to only a negligible change in the current through the field effect transistor, the latter change, in its turn, causing a greater change in the collector current through the transistor and through the resistor Rs, and causing in the said resistor Rs a voltage change of which the magnitude and phase position are practically equal to the voltage change, in the gate, by which it was caused. With this "source follower" arrangement augmented by an amplifier transistor, the considerable advantage is obtained that the voltage between the source and the gate and thus the bias voltage of the photo-diode remain almost constant, completely independently of any photo-electric current flowing through the photo-diode. Similarly, this arrangement considerably improves the linearity of the circuit, since, in order to enable the FET to be driven hard, only a very limited and linear portion of the operating characteristic line is required.

In one advantageous embodiment of the invention a resistor is connected into the drain supply line, between the emitter and the base of the transistor. This resistor, together with the resistor Rs in the source branch, only serves to set the operating point of the FET and of the transistor. Constant voltage values between the source and the gate can be optimated by selecting the right dimensions for the said resistor.

One example of the circuit arrangement covered by the invention will be described hereinafter in greater detail, by reference to a circuit diagram.

For the exact measurement of photo-electric currents with Si-photo-diodes the circuit arrangement is based on the basic connection of a source follower with a field effect transistor (FET) 1. The drain of the FET is connected to the positive pole of a direct voltage source, while the source and the gate are indirectly connected with a negative pole. A photo-diode 4 is connected between the source connection 6 and the gate 12 of the FET 1. Photo-electric current occurring is then measured as a voltage drop in an operating resistor 5 in the supply line of the gate. With a change-over switch 13 it is possible to switch over to further resistance values with corresponding measuring ranges, as indicated by the broken lines in the diagram. A resistor Rs 3 is connected to the source connection 6.

To linearise the circuit arrangement and improve the constancy of the bias voltage in the Si-photo-diode 4 situated between the gate 12 and the source 6 of the FET 1, an additional transistor 2 is connected into the basic circuit of the source follower in such a way that its base is connected to the drain connection 7 while its collector is connected with the source connection 6 of the FET 1. The emitter connection 11 of the additional transistor 2 is directly connected to the positive pole of the voltage source. In order to enable the operating point of the FET 1 and also that of the transistor 2 to be selected at the same time, a resistor 8, in the drain supply line 15, is connected by one end to the drain 7 and to the base 9 and by the other connection to the positive of the voltage source.

One method of operation of the circuit arrangement, illustrating its most essential characteristics in a simplified form, is the following:

If the light falls on the Si-photo-diode 4, this results in a photo-electric current which causes, in the operating resistor 5, a voltage drop which, in turn, leads to a change in the voltage in the gate 12 and thus causes the FET 1 to be driven hard. If, as is the case in the usual source follower circuit, the said voltage change in the gate 12 only causes the FET 1 to be driven hard, i.e. if the source current change in the resistor Rs 3, caused by the voltage change in the gate 12, were compared as a correspondingly altered voltage drop with the magnitude of the voltage prevailing in the gate 12, then a voltage difference would be observed which would be unacceptably high for measuring purposes.

This means that the gate voltage at the connection points of the Si-photo-diode 4, assumes different values with every change in the brightness of the incident light and thus in the photo-electric current through the Si-photo-diode 4. In addition to the non-linear characteristics of the circuit arrangement there are also the unfavourable influences of the intrinsic capacities of Si-photo-diodes, as they restrict its limit frequency. The circuit arrangement thus has a relatively slow response.

To improve the linearity and, above all, to eliminate unfavourable influences of the intrinsic capacities of the Si-photo-diodes 4, an almost completely constant bias voltage in the Si-photo-diode 4 must be ensured. This object is achieved by the inclusion, in the circuit arrangement, of an additional transistor 2, as already described. A resistor 8 used in the drain supply line 15 is dimensioned to ensure an optimum measure of agreement between the voltage values in the gate 12, which are changed by the incidence of light on Si-photo-diode 4, and the voltage values changing in the resistor Rs 3. These additional circuit elements enable the bias voltage in the Si-photo-diode 4 to be kept largely constant. A photo-electric current flowing through the Si-photo-diode 4 as a result of a change in the brightness thus

results in a certain voltage drop in the resistor 5, and a somewhat higher current commences to flow through the FET 1. This current, however, via the base 9, immediately actuates the transistor 2 still further, so that an increased collector current likewise begins to flow. In accordance with the dimensions selected for the circuit this collector current of the transistor 2 flows together with the now very slightly increased source current through the directly connected resistor Rs 3 and is available at the circuit point 14 as a voltage value. The voltage drop thus caused in the resistor Rs 3 by the source current and collector current is so dimensioned that it is almost equal to the voltage value measured in the gate 12. The maximum possible constancy obtained in the bias voltage in the Si-photo-diode 4 is thus mainly brought about by the collector current of the transistor 2. In this case the current through the FET 1 is only required to constitute a very slight proportion. The voltage differences occurring throughout the entire range of the measuring circuit between the voltage values measured in the gate 12 and those measured in the resistor Rs 3 will only amount to a few tenths of one percent in the circuit arrangement constructed according to the invention, so that the bias voltage in the Si-photo-diode 4 can also be regarded as sufficiently constant for high-quality brightness measuring operations. With circuit arrangements hitherto customary, operating without the additional linearisation transistor 2, on the other hand, the voltage differences found amounted to a few percent. Such values, as already explained in detail, are unsuitable for high-quality measuring operations.

WHAT WE CLAIM IS:—

1. A photo-diode circuit arrangement for the amplification of photo-electric current, comprising: a field effect transistor connected on the "source follower" principle, a photo-diode connected between source and gate of said field effect transistor and a pnp transistor the base of which being connected with the drain and the collector with a source connection of the field effect transistor and the emitter of which being connected to the drain supply line.

2. A photo-diode circuit as claimed in claim 1, wherein a resistor is connected into the drain supply line between the emitter connection and the base connection of the transistor.

3. A photo-diode circuit arrangement, substantially as described herein with reference to and as illustrated by the accompanying drawing.

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